Public Products List

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PCN Title : Power Management BU: Alternative die for TL431AIL3T and TL432AIL3T

PCN Reference : AMS/21/13153

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

TL431AIL3T	TL432AIL3T	

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Reliability

Voltage References

New Product qualification

TL431BL3T

M43101 Line
Technology HBIP40V
Package SOT23 3 L

General Information	
Product Lines	*M43101*
Product Description	Programmable voltage reference
P/N	TL431BL3T
Product Group	*AMG*
Product division	*General Purpose Analog & RF Division*
Package	*SOT23 3 L / SO8*
Silicon Process technology	*HBIP40*

Locations	
Wafer fab	*Singapore 6*
Assembly plant	*Carsem / Shenzhen*
Reliability Lab	*Catania Reliability LAB*

DOCUMENT INFORMATION

Version	Date	Pages	Handled by	Approved by	Comment
1	August 2020	6	Angelo.Basile	Giuseppe Giacopello	Final Report

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW OBJECTIVES

To qualify the New Product TL431BL3T

4 CONCLUSION

The present reliability results are positive.

5 DEVICE CHARACTERISTIC

5.1 Device description

The TL431 is an adjustable shunt voltage reference with guaranteed temperature stability over the entire operating temperature range .the operating output voltage may be set any value between 2.5 and 36V with two impedenca external resistors.The TL431operates with a wide current range from 1 to 100mA with a typical dynamic impedence of 0.2

5.2 Construction note

P/N	TL431	
Wafer/Die fab. information		
Wafer fab manufacturing location	Singapore AMK6	
Technology	HBIP40V	
Die finishing back side	Lapped Silicon	
Die size	830 x 780 micron	
Wa fer Passivation type	PVAPOX-NITRIDE	
Assembly information		
Assemby Site	Carsem M	SHENZHEN B/E
Package description	SOT23 3 L	SO8
Molding compound	Epoxy	Epoxy
Frame	HDLF NiPdAu	NiThPdAgAu
Die attach material	Epoxy	Epoxy
Wires bonding materials/diameters	1 mils Cu	1 mils Cu
Final testing information		
Testing location	Carsem S	SHENZHEN B/E
Tester	ASL1000	
Test program	M431 1	M431_STS_01

6 TEST VEHICLE & TEST PLAN

Lot #	Diffusion Lot	Assy Lot	Package	Product Line	Comments
1	V6010VYY	E016A11	SOT23 3L	M43101	
2	6208FFJH32	9Y233ADH	SOT23 3L	M43101	
3	60197XV	GK2320LN	SO8		

Test	PC	Std ref.	Conditions		Steps	Failure/SS			Generic Data For Voltage Reference
						1° Lot SOT23-3L	2° Lot SOT23-3L	3° Lot SO8	
Silicon related									
HTOL	N	JESD22 A-108	Tj = 125° C, Vbias=+5V	77	168 h	0/77		0/77	0/308 (77x4lot)
					500 h	0/77		0/77	
					1000 h	0/77		0/77	
HTSL	N	JESD22 A-103	Ta = 150° C	45	168 h	0/45	0/45	0/45	0/180 (45x4lot)
					500 h	0/45	0/45	0/45	
					1000 h	0/45	0/45	0/45	
Package related									
PC		JESD22 A-113	Driving 24 h @125°C store 168h @ Ta=85°C Rh = 85 % Oven Reflow @ Tpeak=260°C 3 times	231	Final	PASS	PASS	PASS	
AC	Y	JESD22 A-102	Ta = 121°C, Pa = 2 Atm	77	168h	0/77	0/77	0/77	0/308 (77x4lot)
						0/77	0/77	0/77	
						0/77	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65° C to 150° C	77	100 cy	0/77	0/77	0/77	0/308 (77x4lot)
					200 cy	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85° C, RH = 85%, Vbias=+2.5V	77	168 h	0/77	0/77	0/77	0/308 (77x4lot)
					500 h	0/77	0/77	0/77	
					1000 h	0/77	0/77	0/77	
Other Tests									
ESD	N	JESD22-A114	HBM	3	2KV		PASS	PASS	
		JESD22-C101	CDM	3	1.5KV			PASS	

Note: All samples are assembly on dedicated PCB in agreement with JEDEC020

7 TEST DESCRIPTION

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other Test		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. **CDM**: Charged Device Model **HBM**: Human Body Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.